WHAT IS CLAIMED IS:

1. A stabilized power supply circuit comprising:

a charge pump power supply circuit including a plurality of switches and a capacitor, wherein, through combination of selective on and off operations of the individual switches, the charge pump power supply circuit accumulates electric charge in the capacitor and outputs, as output voltage, voltage generated upon accumulation of electric charge; and

an error amplifier comparing the output voltage and a predetermined reference voltage and outputting an error signal on the basis of the difference between the output voltage and the reference voltage, wherein

at least one of the switches of the charge pump power supply circuit is constituted by a field effect transistor; and a period during which electric charge is charged into or discharged from a gate of the field effect transistor is controlled in accordance with the error signal in order to maintain the output voltage constant.

2. A stabilized power supply circuit according to claim 1, wherein a current source is connected in series to the gate of the field effect transistor; and the period during which electric charge is charged into or discharged from the gate is controlled by controlling the current source in accordance with the error signal output from the error amplifier.

3. A stabilized power supply circuit according to claim 2, wherein the current source is formed of a transistor.

4. A stabilized power supply circuit according to claim 3, wherein the current source is formed of a MOS-type field effect transistor.

5. A stabilized power supply circuit comprising:

a charge pump power supply circuit including a plurality of switches and a capacitor, wherein, through combination of selective on and off operations of the individual switches by means of clock pulses, the charge pump power supply circuit accumulates electric charge in the capacitor and outputs, as output voltage, voltage generated upon accumulation of electric charge; and

an error amplifier comparing the output voltage and a first reference voltage and outputting an error signal on the basis of the difference between the output voltage and the first reference voltage, wherein

at least one of the switches of the charge pump power supply circuit is controlled in accordance with the error signal in order to maintain the output voltage constant; and

the voltage of the error signal is compared with a second reference voltage, and when the difference between the voltage of the error signal and the second reference voltage is equal to or less than a predetermined value, the charge

pump operation performed through selective on and off operations of the individual switches by means of the clock pulses is stopped.

6. A stabilized power supply circuit comprising:

a charge pump power supply circuit including a plurality of switches and a capacitor, wherein, through combination of selective on and off operations of the individual switches by means of clock pulses, the charge pump power supply circuit accumulates electric charge in the capacitor and outputs, as output voltage, voltage generated upon accumulation of electric charge; and

an error amplifier comparing the output voltage and a first reference voltage and outputting an error signal on the basis of the difference between the output voltage and the first reference voltage, wherein

at least one of the switches of the charge pump power supply circuit is constituted by a field effect transistor; and a period during which electric charge is charged into or discharged from a gate of the field effect transistor is controlled in accordance with the error signal in order to maintain the output voltage constant; and

the voltage of the error signal is compared with a second reference voltage, and when the difference between the voltage of the error signal and the second reference voltage is equal to or less than a predetermined value, the charge pump operation performed through selective on and off

operations of the individual switches by means of the clock pulses is stopped.

7. A stabilized power supply circuit according to claim 6, wherein a current source is connected in series to the gate of the field effect transistor; and the period during which electric charge is charged into or discharged from the gate is controlled by controlling the current source in accordance with the error signal output from the error amplifier.

8. A stabilized power supply circuit according to claim 7, wherein the current source is formed of a transistor.

9. A stabilized power supply circuit according to claim 8, wherein the current source is formed of a MOS-type field effect transistor.